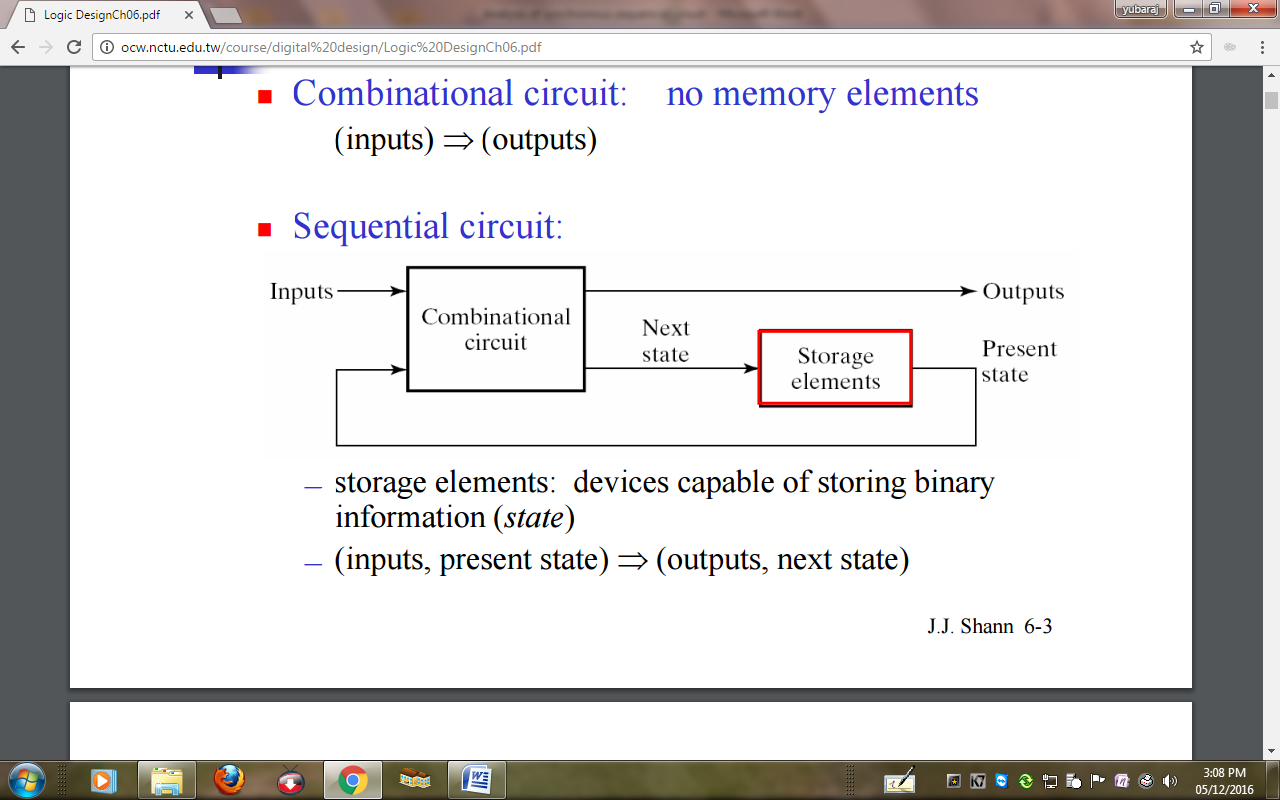
* Combinational circuit: no memory elements (inputs) ⇒ (outputs)



**Types of Sequential Circuits**

1. Synchronous seq. ckt: – Its behavior can be defined from the knowledge of its signals at discrete instants of time. – Storage elements: e.g., flip-flops
2. Asynchronous seq ckt: – Its behavior depends upon the input signals at any instant of time and the order in which the inputs change. – Storage elements: e.g., latches, feedback paths – Disadvantage: may be unstable & difficult to design

**Synchronous Sequential Circuits**

* Clocked seq ckts is the most commonly used sync seq ckts is syn seq ckts .
* They use clock pulses in the inputs of storage elements
* It has a master-clock generator to generate a periodic train of clock pulses ¾

- The clock pulses are distributed throughout the system. ¾

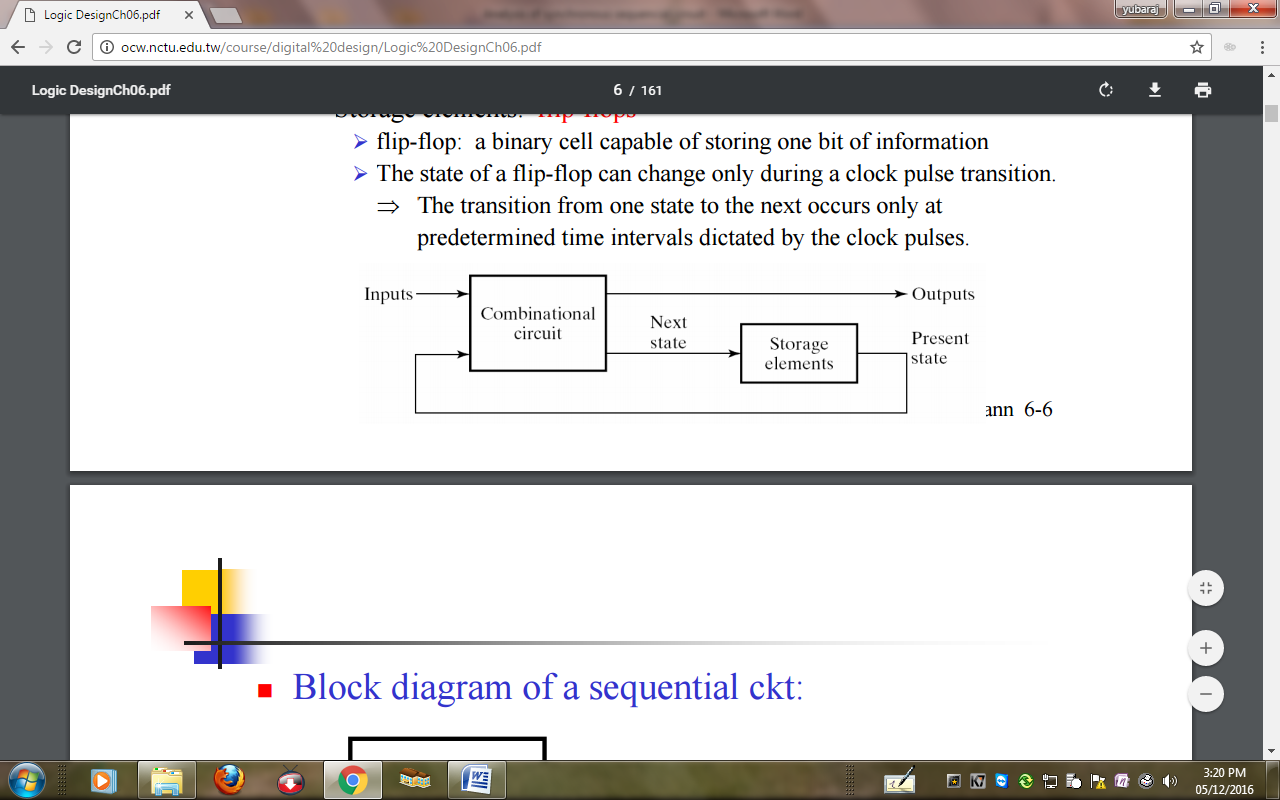
- Storage elements are affected only w/ the arrival of each pulse.

* Adv.: seldom manifest instability problems
* Storage elements: flip-flops

- Flip-flop: a binary cell capable of storing one bit of information

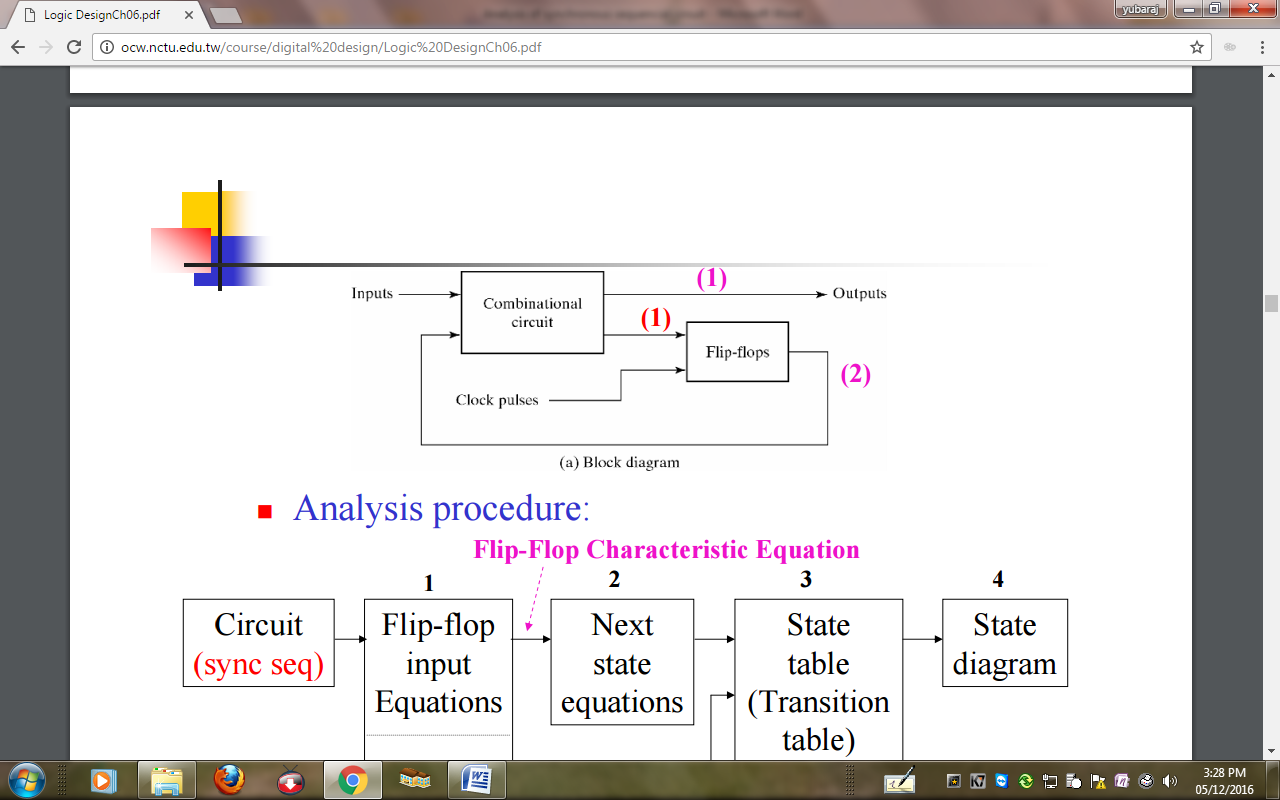
- The state of a flip-flop can change only during a clock pulse transition.

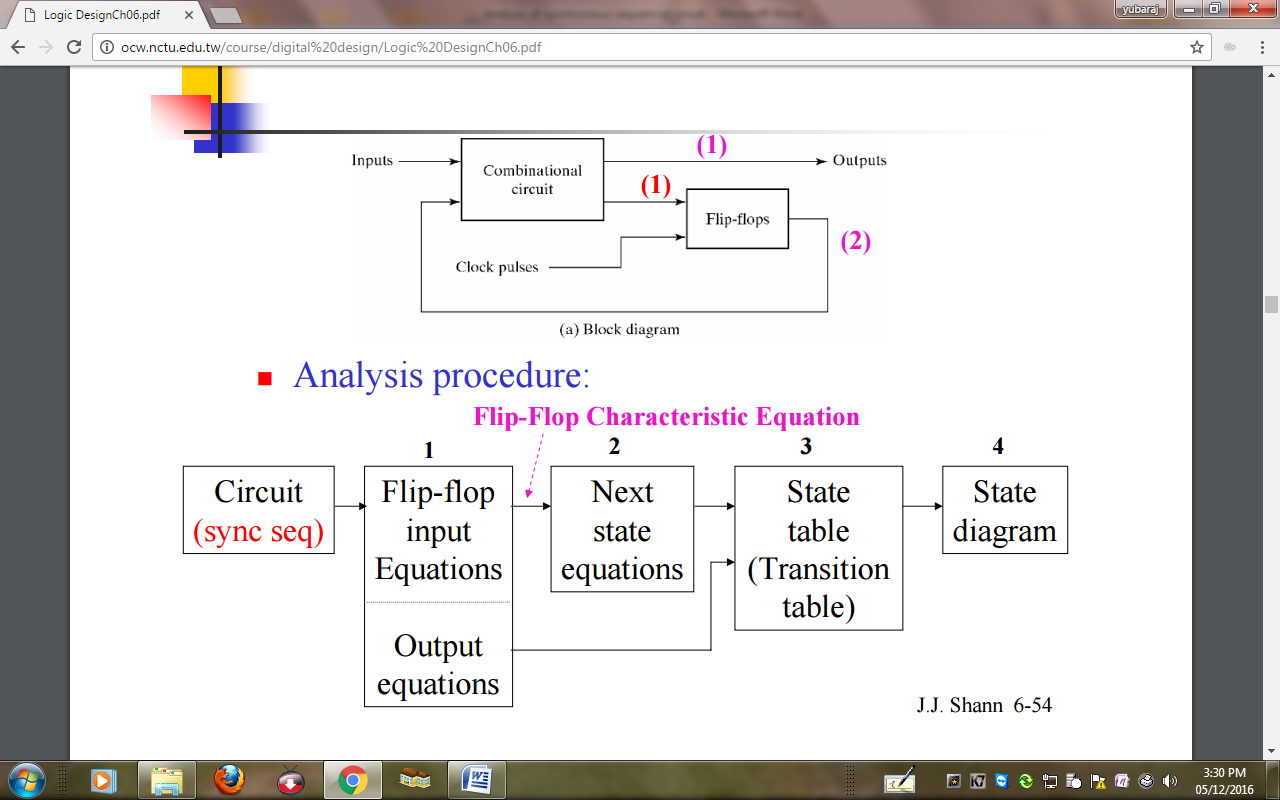
⇒ The transition from one state to the next occurs only at predetermined time intervals dictated by the clock pulses.



**(Sync) Sequential Circuit Analysis**

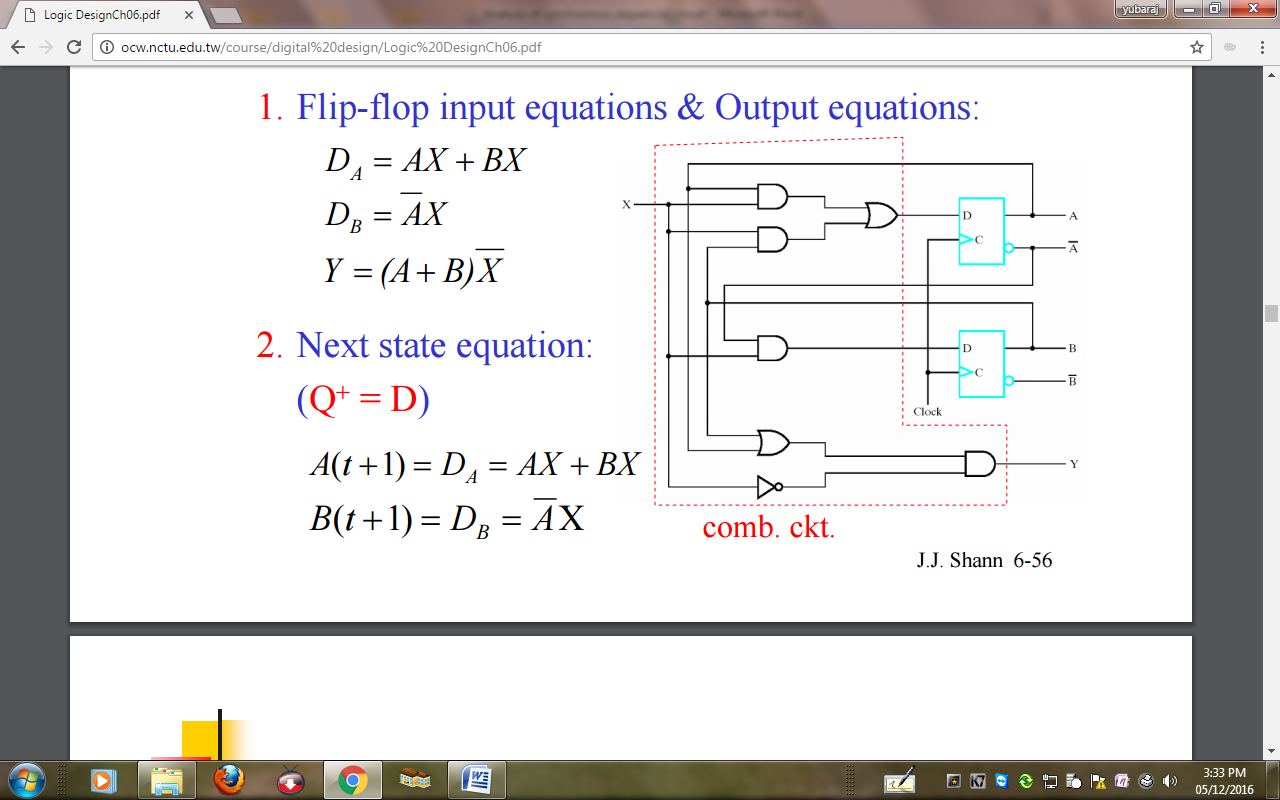
* Synchronous seq ckt: — includes f-fs, the clock inputs driven directly or indirectly by a clock signal and the direct sets and resets are unused during the normal functioning of the ckt
* The behavior of a seq ckt is determined from the inputs, outputs, and present state of the ckt. 
* Analysis of a seq ckt: — obtain a suitable description that demonstrates the time sequence of inputs, outputs, and states.

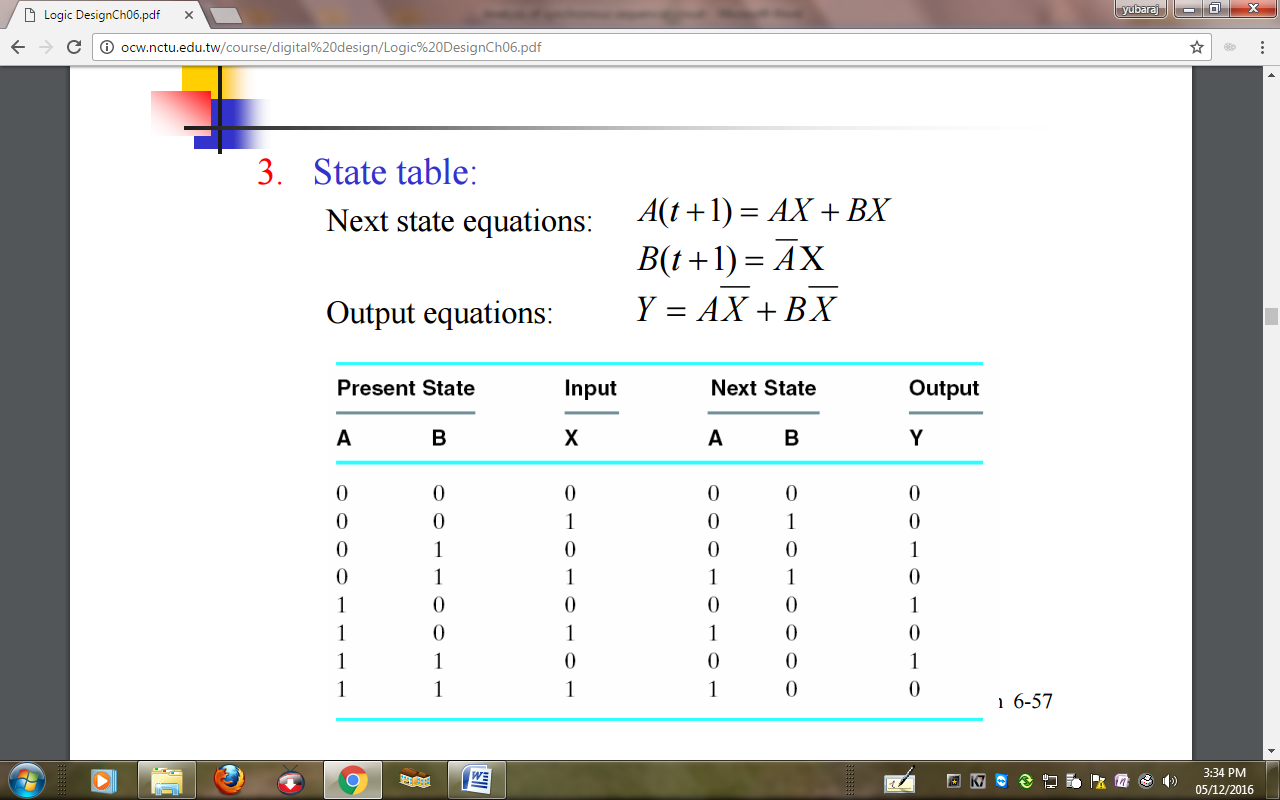
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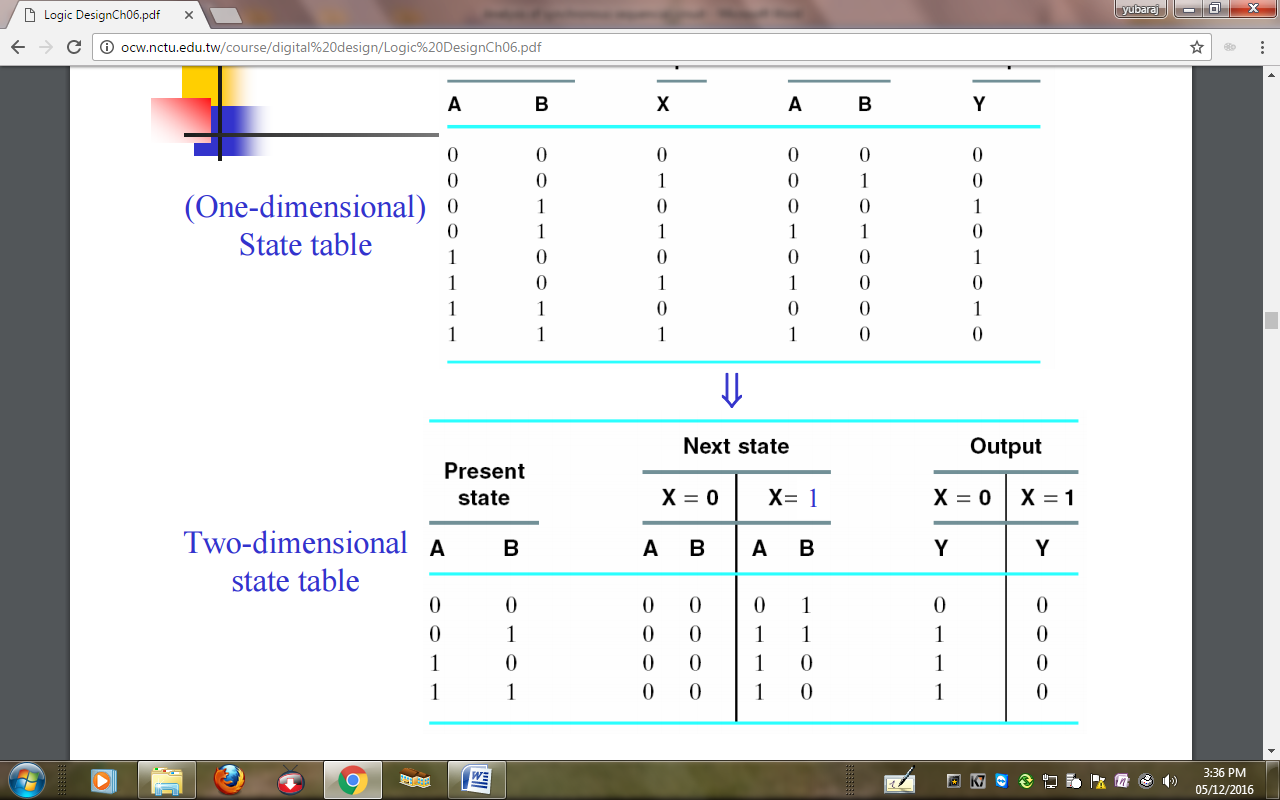
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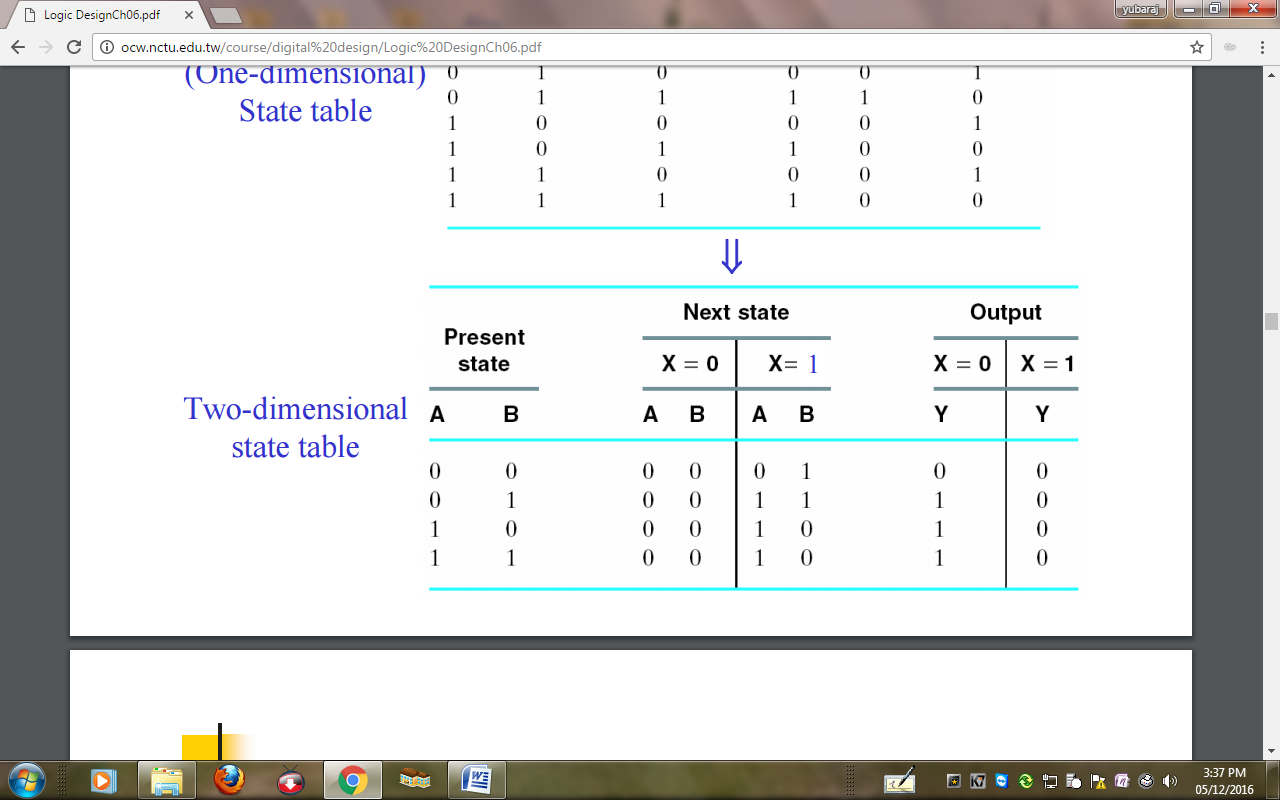
**Analysis w/ D Flip-Flops**

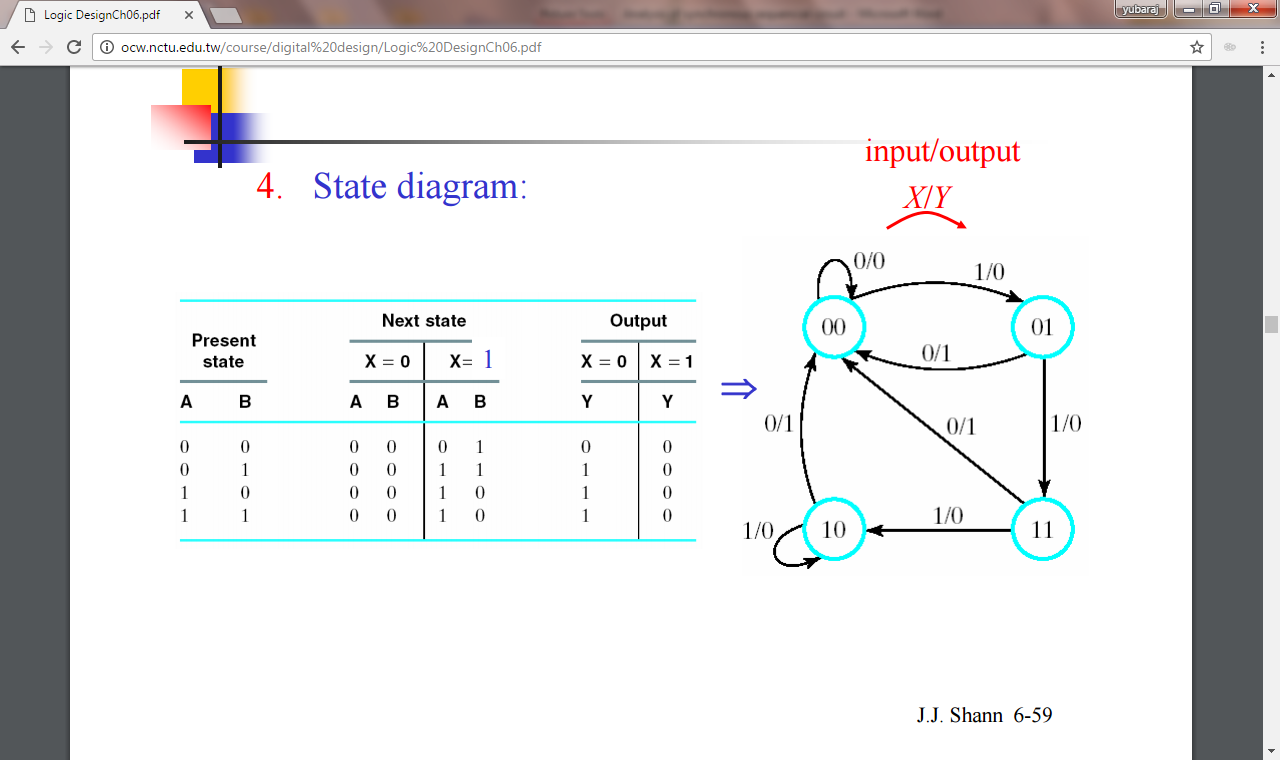
**Example 1.**

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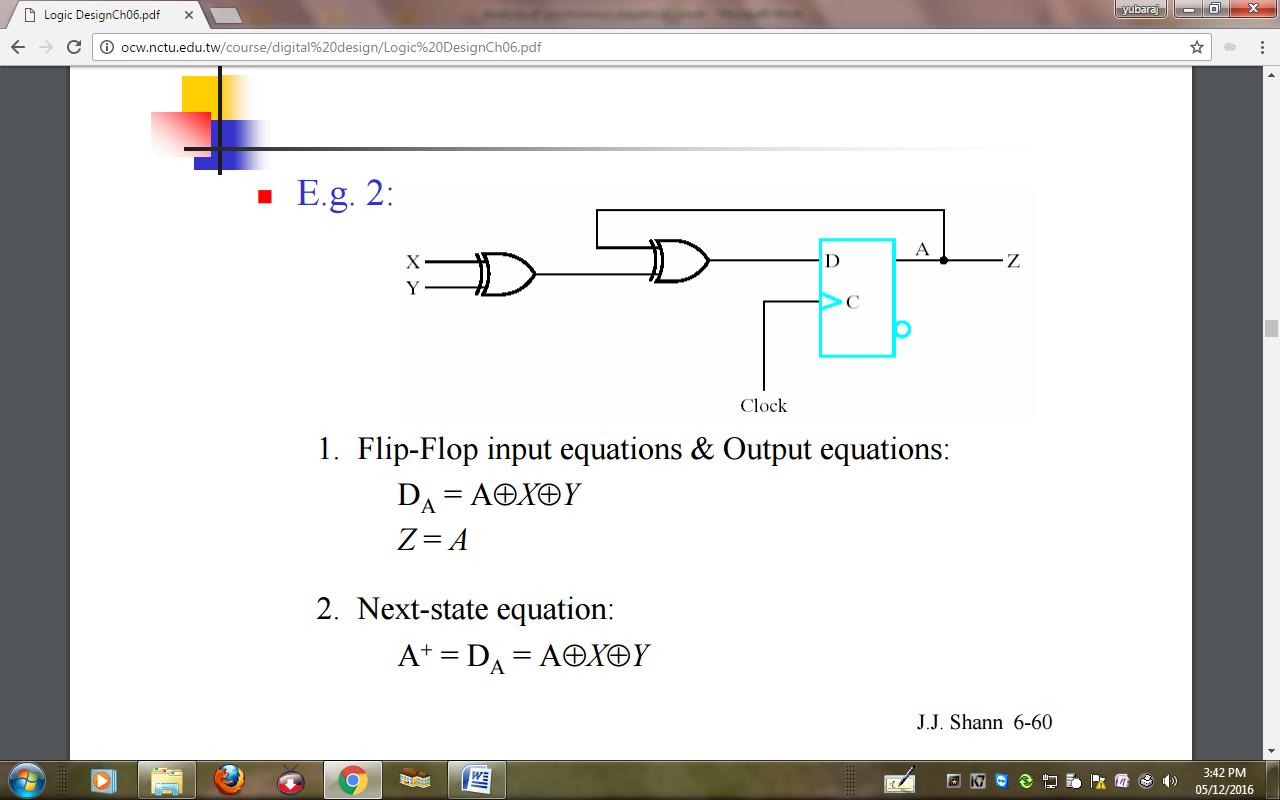
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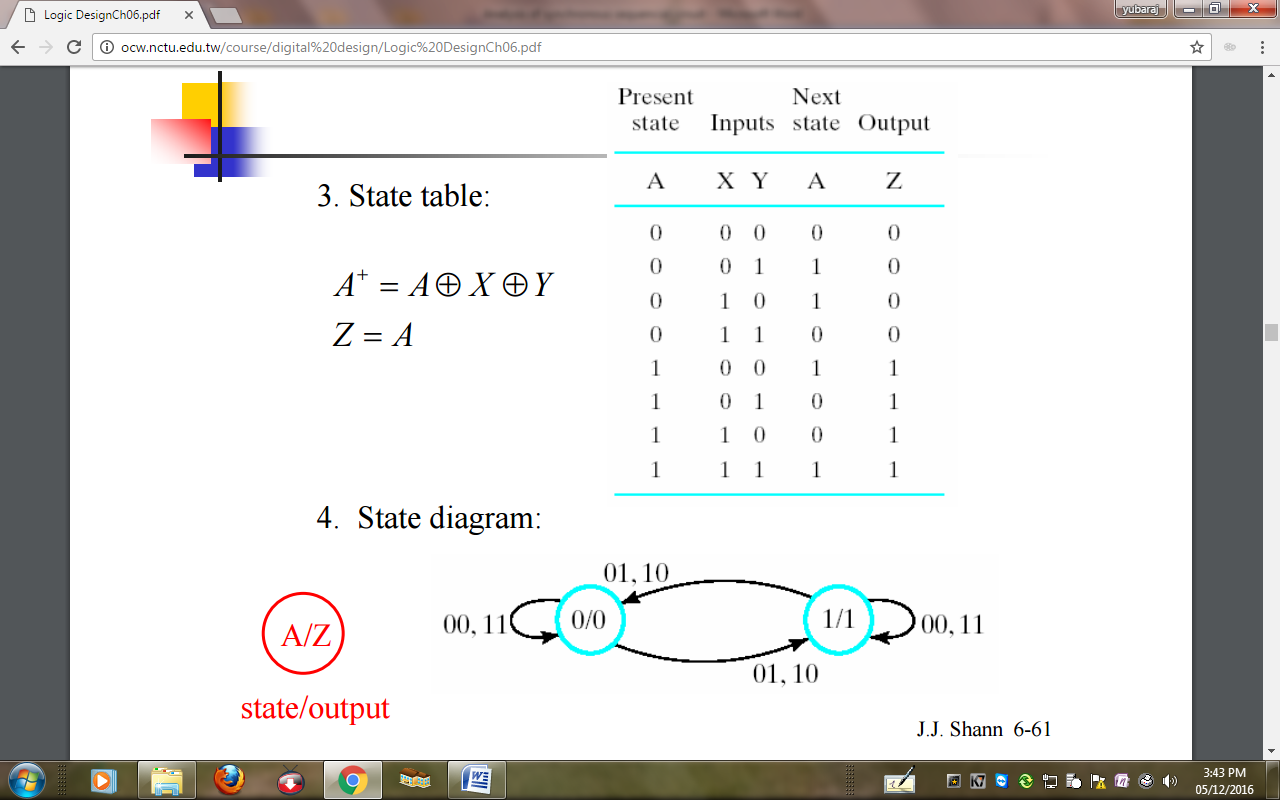
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**Example 2.**

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***Analysis JK Flip-Flops***

***(Analysis of J/k Flip flops and T flip-flops is also done applying the same steps.)***

(**Sync) Sequential Circuit Design**

The following steps /procedural steps are undertaken for the designing of the synchronous sequential Circuit:

1. **Specification**: Writing a specification for the ckt.
2. **Formulation**: Obtain either a state diagram or state table from the statement of the problem.

\* State reduction: Reduce the # of states if necessary.

1. **State assignment**: Assign binary codes to the states and obtain the binary-coded state table.
2. **Flip-flop input equation determination**: Select the flip-flop type or types. Derive the flip-flop input equations from the next-state entries in the encoded state table.
3. **Output equation determination**: Derive output equations from the output entries in the state table.
4. **Optimization**: Optimize the flip-flop input equations and output equations.
5. **Technology mapping**: Draw a logic diagram of the ckt using flip-flops, ANDs, ORs, and inverters. Transform the logic diagram to a new diagram using the available flip-flop and gate technology.
6. **Verification**: Verify the correctness of the final design.